Claims

What is claimed is:

1. A power amplifier configuration comprising:
   a) power control circuitry including a power regulator providing an output voltage at an output node responsive to an adjustable power control signal; and
   b) power amplifier circuitry including an input amplifier stage in series with an output amplifier stage for amplifying a radio frequency input signal, the input amplifier stage receiving power from a fixed voltage node and the output amplifier stage receiving power via the output node of the power regulator;

   wherein the adjustable power control signal is adjusted to control output power provided by the power amplifier circuitry by controlling the voltage supplied to the output amplifier stage.

2. The power amplifier configuration of claim 1 further comprising bias circuitry for providing a constant bias to the input and output amplifier stages.

3. The power amplifier configuration of claim 1 wherein the power regulator is a voltage regulator.

4. The power amplifier configuration of claim 3 wherein the power regulator is a linear closed loop voltage regulator.

5. The power amplifier configuration of claim 1 wherein the power control circuitry further comprises:
   a) an error amplifier having a first input for receiving the adjustable power control signal, a second input, and an output coupled to the power regulator to control the output voltage at the output node; and
   b) a feedback network coupled between the output node of the power regulator and the second input of the error amplifier;

wherein the output of the error amplifier is responsive to both the adjustable power control signal and a voltage signal fed back from the output node of the power regulator.

6. The power amplifier configuration of claim 1 wherein the power amplifier circuitry further comprises a second output amplifier stage between and in series with the input and output amplifier stages, the second output amplifier stage receiving power via the output node of the power regulator such that the adjustable power control signal is adjusted to control output power provided by the power amplifier circuitry by controlling the voltage supplied to the output amplifier stage and the second output amplifier stage.

7. The power amplifier configuration of claim 6 wherein the bias circuitry further provides a constant bias to the second output amplifier stage.

8. A mobile terminal comprising:
   a) a control system providing an adjustable power control signal to control output power for transmitted radio frequency signals;
   b) communication electronics associated with the control system and comprising:
      i) power control circuitry including a power regulator providing an output voltage at an output node responsive to an adjustable power control signal; and
      ii) power amplifier circuitry including an input amplifier stage in series with an output amplifier stage for amplifying a radio frequency input signal, the input amplifier stage receiving power from a fixed voltage node and the output amplifier stage receiving power via the output node of the power regulator;

   wherein the adjustable power control signal is adjusted to control output power provided by the power amplifier circuitry by controlling the voltage supplied to the output amplifier stage.

9. The mobile terminal of claim 8 further comprising bias circuitry for providing a constant bias to the input and output amplifier stages.

10. The mobile terminal of claim 8 wherein the power regulator is a voltage regulator.

11. The mobile terminal of claim 10 wherein the power regulator is a linear closed loop voltage regulator.

12. The mobile terminal of claim 8 wherein the power control circuitry further comprises:

a) an error amplifier having a first input for receiving the adjustable power control signal, a second input, and an output coupled to the power regulator to control the output voltage at the output node; and

b) a feedback network coupled between the output node of the power regulator and the second input of the error amplifier;

wherein the output of the error amplifier is responsive to both the adjustable power control signal and a voltage signal fed back from the output node of the power regulator.

13. The mobile terminal of claim 8 wherein the power amplifier circuitry further comprises a second output amplifier stage between and in series with the input and output amplifier stages, the second output amplifier stage receiving power via the output node of the power regulator such that the adjustable power control signal is adjusted to control output power provided by the power amplifier circuitry by controlling the voltage supplied to the output amplifier stage and the second output amplifier stage.

14. The mobile terminal of claim 13 wherein the bias circuitry further provides a constant bias to the second amplifier output stage.

15. The mobile terminal of claim 8 wherein the adjustable power control signal is V_{RAMP}.

16. A semiconductor implementing a power amplifier configuration comprising:
    a) power control circuitry including a power regulator providing an output voltage at an output node responsive to an adjustable power control signal; and
    b) power amplifier circuitry including an input amplifier stage in series with an output amplifier stage for amplifying a radio frequency input signal, the input amplifier stage receiving power from a fixed voltage node and the output amplifier stage receiving power via the output node of the power regulator;

    wherein the adjustable power control signal is adjusted to control output power provided by the power amplifier circuitry by controlling voltage supplied to the output amplifier stage.

17. The semiconductor of claim 16 further comprising bias circuitry for providing a constant bias to the input and output amplifier stages.

18. The semiconductor of claim 16 wherein the power regulator is a voltage regulator.

19. The semiconductor of claim 18 wherein the power regulator is a linear closed loop voltage regulator.

20. The semiconductor of claim 16 wherein the power control circuitry further comprises:
    a) an error amplifier having a first input for receiving the adjustable power control signal, a second input, and an output coupled to the power regulator to control the output voltage at the output node; and
    b) a feedback network coupled between the output node of the power regulator and the second input of the error amplifier;

wherein the output of the error amplifier is responsive to both the adjustable power control signal and a voltage signal fed back from the output node of the power regulator.

21. The semiconductor of claim 16 wherein the power amplifier circuitry further comprises a second output amplifier stage between and in series with the input and output amplifier stages, the second output amplifier stage receiving power via the output node of the power regulator such that the adjustable power control signal is adjusted to control output power provided by the power amplifier circuitry by controlling voltage supplied to the output amplifier stage and the second output amplifier stage.

22. The semiconductor of claim 21 wherein the bias circuitry further provides a constant bias to the second amplifier output stage.

23. A method comprising:
    a) providing a regulated output voltage responsive to an adjustable power control signal;
    b) providing an input amplifier stage in series with an output amplifier stage for amplifying a radio frequency input signal;
    c) providing power to the input amplifier stage from a fixed voltage node; and
    d) providing power to the output amplifier stage via the regulated output voltage;

    wherein the adjustable power control signal is adjusted to control output power provided by controlling voltage supplied to the output amplifier stage.

24. The method of claim 23 further comprising providing a constant bias to the input and output amplifier stages.

25. The method of claim 23 further comprising:
    a) providing feedback from the regulated output voltage; and

b) generating a voltage control signal to control the regulated output voltage responsive to both the adjustable power control signal and feedback from the regulated output voltage.

26. The method of claim 23 wherein the amplifier circuitry further comprises providing a second output amplifier stage between and in series with the input and output amplifier stages, the second output amplifier stage receiving power via the output node of the power regulator such that the adjustable power control signal is adjusted to control output power provided by the power amplifier circuitry by controlling voltage supplied to the output amplifier stage and the second output amplifier stage.

27. The method of claim 26 further comprising providing a constant bias to the second amplifier output stage.